

DETAILED ACTION

Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

2. Replace the Abstract with the following:

A memory system including large-capacity ROM and RAM in which high-speed reading and writing are enabled is provided. A memory system including a non-volatile memory (CHIP1), DRAM (CHIP3), a control circuit (CHIP2) and an information processing device (CHIP4) is configured. Data in FLASH is transferred to SRAM or DRAM in advance to speed up. Data transfer between the non-volatile memory (FLASH) and DRAM (CHIP3) can be performed in the background. The memory system including these plural chips is configured as a memory system module in which each chip is mutually laminated and each chip is wired via a ball grid array (BGA) and bonding wire between the chips. Data in FLASH can be read at the similar speed to that of DRAM by securing a region in which the data in FLASH can be copied in DRAM and transferring the data to DRAM in advance immediately after power is turned on or by a load instruction.

3. Authorization for this examiner's amendment was given in a telephone interview with Patrick Miller [Reg.No.57,502] on 16 June 2009.

4. In the claims, the following amendments are to be made:

Claim 25, last line, after "the access", insert --from the second control circuit--.

Claim 79, line 3, after "memory", insert --from outside the memory module--.

Statement of Reasons for Allowance

5. The following is an examiner's statement of reasons for allowance:

No known prior art teaches the combination of these features: 1) a memory module including a non-volatile memory, a DRAM, a SRAM, and a first control circuit accessing the non-volatile memory, the DRAM and the SRAM; 2) a DRAM interface connected to a first memory controller outside the memory module for accessing the DRAM from outside the memory module and a SRAM interface connected to a second memory controller outside the memory module different from the first memory controller for accessing the SRAM from outside the memory module; 3) the first control circuit receiving first instruction for transferring data from the non-volatile memory to the DRAM through the DRAM interface and second instruction for transferring data from the non-volatile memory to the SRAM through the SRAM interface.

As the Applicant had pointed out in the response filed 4 June 2009, the Hiraki reference does not teach the first control circuit, the first memory controller, and the second memory controller that is different from the first memory controller. If Hiraki's Control circuit 20 and CPU 10 (see Hiraki, Fig. 17) are considered to be the first and second memory controllers outside the memory module, then CPU 10 cannot be part of the first control circuit because the first control circuit must be within the memory module. On the other hand, it may be better to consider Hiraki's CPU 10 as the first control circuit because it is responsible for processing instructions from the non-volatile memory, the DRAM and the SRAM and for transferring data from the nonvolatile memory to the DRAM and the SRAM (see Hiraki, col. 10, lines 25-43 and col. 11, lines 36-39 and 57-63). But it would be inconsistent to consider CPU 10 as both the first control circuit which is included by the memory module and the second memory controller which is outside of the memory module. Hiraki's CPU 10 can only take the role of one of the two (first control circuit and second memory controller) and Hiraki does not teach another component that can supplement CPU 10 and act as either the first control circuit or the second memory controller.

A newly discovered reference, Kim et al. [US 2001/0015905 A1], teaches a microprocessor including a separate controller for each of a Flash memory, a DRAM and a SRAM (see Kim et al., Fig. 1 and [0003]-[0005]). However, Kim et al. does not teach a memory module including a non-volatile memory, a DRAM and a SRAM, as well as a first control circuit that receives instructions to transfer data between the non-volatile memory, the DRAM and the SRAM. Kim et al. also fails to teach first and

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second memory controllers outside the memory module. Kim et al.'s controllers are in the same microprocessor/control circuit which receives instructions to transfer data between the non-volatile memory, the DRAM and the SRAM.

Also note that the Abstract has been amended by this Examiner because it was not limited to a single paragraph and the last paragraph referred to purported merits or speculative applications of the invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/SHAWN X GU/

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Patent Examiner
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16 June 2009

/Reginald G. Bragdon/
Supervisory Patent Examiner, Art Unit 2189